IN THE SPECIFICATION:

Page 7:

Please substitute the following paragraph for the paragraph beginning at line 10:

B1

Due to this, as shown in FIG. 50, when a silicon nitride film 108 serving as a sidewall insulating film is deposited on the semiconductor substrate 100 in the next step, stepped portions are generated on the silicon nitride film 108 in the vicinity of respective boundaries between each control gate electrode 104 and the silicon oxide film 105. As a result, when contact holes are formed in the space regions of the gate electrodes (floating gate electrodes 102 and control gate electrodes 104) by means of the SAC technique, the silicon nitride film 108 on each stepped portion described above is removed and thickness thereof becomes thin. Thereafter, a problem of defects has occurred such that a metal film embedded into each contact hole and the control gate electrode 104 become closer to each other in the vicinity of each stepped portion described above, and both become short-circuit according to circumstances. The problem like this arises even in the case where the protection insulating film covering the upper portion of each control gate electrode 104 is formed

B

B1 of a laminating film consisting of a silicon oxide film and a silicon nitride film.

Page 8:

Please substitute the following paragraph for the paragraph beginning at line 2:

B2 As stated above, by consideration of the inventors, it has become clear that if a part of or all of the protection insulating film covering the upper portion of each control gate electrode is formed of a silicon oxide film in order to suppress stress of the gate oxide film and the substrate of the lower portion thereof, the stress being resulted from the silicon nitride film, then it is extremely difficult to realize the micro-fabrication of the MISFET by utilizing the SAC technique.

IN THE CLAIMS:

Please cancel Claims 1-10 without prejudice or disclaimer.

B3 1. ~~11.~~ (Amended) A method for manufacturing a semiconductor integrated circuit device including a MIS transistor structure, the method comprising the steps of: